

ADVANCED GRID-CONNECTED MULTILEVEL INVERTER WITH REDUCED COMPONENTS AND ENHANCED POWER QUALITY FOR RENEWABLE ENERGY APPLICATIONS

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ABSTRACT

Grid-interfaced renewable-energy systems require power electronic converters that deliver high waveform quality with low semiconductor stress and low component count. The cross-connected multilevel inverter (CC-MLI) recently reported by Pathak et al. is an attractive reduced-device-count baseline: it produces nine single-phase output levels using only eight semiconductor switches, four capacitors and two DC sources, without a polarity-changing H-bridge, and it has been validated in MATLAB/Simulink for a standalone 24 V + 24 V laboratory-scale load. Three measurable limitations motivate this work: the nine-level resolution caps the low-order staircase total harmonic distortion (THD) of the output voltage at approximately 11.5 % at a modulation index of 0.85 (analytically derived in this paper); the capacitor self-balancing property is asserted but neither modelled nor proven; and no grid-connected control, filtering, synchronization or robustness study is presented. This paper develops a single, verifiable advancement over that baseline: an asymmetric-ratio cross-connected multilevel inverter (AsCC-13L) for grid-connected renewable-energy applications. By re-rating the right-hand module of the unchanged eight-switch skeleton to $V_2 = 2 \cdot V_1$, the identical hardware eight switches, four capacitors, two DC sources synthesises thirteen equidistant voltage levels of step $V_1/2$, lowering the analytically-derived staircase THD floor to approximately 7.1 % at the same modulation

index while preserving the total-standing-voltage-to-peak-output ratio of 4.5 and the count of three conducting devices per state. A charge-integral analysis proves that, under the proposed state assignment, the per-fundamental-cycle net charge drawn from each capacitive divider midpoint is identically zero for any power factor; hence the baseline's self-balancing property survives the asymmetrisation exactly. A complete grid-connected design is additionally developed: dwell-integral capacitor sizing, POD-based level-shifted PWM with a 13-entry switching decoder, perturb-and-observe MPPT, a second-order-generalized-integrator phase-locked loop, decoupled dq-frame PI current control, and a passively damped LCL filter dimensioned by the standard per-unit design rules, together with a ten-case robustness and comparison framework. Numerical THD, efficiency and robustness validation requires MATLAB/Simulink simulation or experimental measurement and is not inferred here; the derived models, state tables, sizing equations and control design constitute the independently checkable technical content of this paper.

Keywords: *Multilevel inverter (MLI)¹, Cross-connected topology², Asymmetric DC sources³, Capacitor voltage balancing⁴, Total standing voltage⁵, Total harmonic distortion⁶, LS-PWM⁷, LCL filter⁸, SOGI-PLL⁹, Grid-connected inverter¹⁰, Photovoltaic systems¹¹, Renewable energy¹².*

1. INTRODUCTION

The accelerating penetration of renewable energy into power systems is driven by distributed photovoltaic (PV) generation, fuel-cell units, small wind and hybrid storage, and each of these sources reaches the ac collection network or the utility grid through a power-electronic interface. At the residential and commercial scale (one to tens of kilowatts, low voltage), the single-phase grid-connected inverter is the standard gateway, and international interconnection standards IEEE Std 1547 for interconnection requirements and IEEE Std 519 for harmonic control at the point of common coupling impose quantitative waveform-quality constraints (grid-current THD below 5 % under the standard's short-circuit ratio assumptions, constraint on even and odd harmonic orders, power-factor and anti-islanding requirements) that the converter must demonstrably meet [15], [16].

Multilevel inverters (MLIs) address these constraints by synthesising the ac waveform as a staircase of discrete voltage levels sourced from segmented dc links, so that each semiconductor device switches only a fraction of the total voltage, the harmonic energy is redistributed to reduced magnitudes and higher orders, and the waveform's distance from a sinusoid falls with every added level [2], [3], [17]. This allows smaller ac filters, lower dv/dt stress on insulation and leakage paths, lower electromagnetic interference and higher effective utilisation of silicon advantages that are decisive exactly for renewable interfaces, where efficiency, lifetime and compliance determine levelised cost of energy.

The three classical MLI families each pay for this in a specific currency. The cascaded H-bridge (CHB) requires a dedicated isolated dc source per cell for thirteen levels, three cells and twelve switches under binary asymmetry, and still a polarity management overhead so the number of isolated sources, each potentially an MPPT-tracked PV string, dominates cost and footprint [3], [10]. The neutral-point-clamped (NPC) converter replaces sources with clamping diodes but the device count and the dc-link balancing burden grow rapidly with levels. The flying-capacitor (FC) converter replaces them with capacitors whose pre-charge, ripple current and balancing dynamics multiply with levels. For low-voltage distributed generation, all three are structurally oversized.

A decade of reduced-switch-count (RSC) and reduced-device-count MLI research has therefore pursued a different contract: keep the harmonic benefits while cutting switches, gate drivers, sources and capacitors, and preferably while generating negative levels without a full-bridge polarity stage [2], [3], [10], [17]–[20]. Switched-capacitor variants additionally bought voltage boost at the price of dynamically charged, load-dependent capacitor voltages [2], [4], [5]; cross-connected source arrangements bought inherent bipolarity at modest switch counts [1], [7]; asymmetric source ratios bought more levels per source, with the ratio 1:3 widely used and the ratio 1:2 generally avoided in the CHB-derived literature because it duplicates levels there [6], [10].

Within this landscape, the CC-type topology of [1] (analysed in depth in Section 2-2.4 of this paper) is a genuinely economical design: eight switches (six unidirectional, two bidirectional), four capacitors arranged as two fixed divider pairs, two equal dc sources, nine levels, bipolar output without an H-bridge, a state-dependent self-balancing assertion for the capacitors, and level-shifted (POD) PWM validated in MATLAB/Simulink at 48 V with a 20 Ω / 20 mH load. Its comparative strength is component-count simplicity per bipolar level.

Precise decoding and enumeration of the baseline (Section 2-2.4) exposes three specific, measurable deficits, none of them generic: **(L1)** nine levels mean an analytically computable low-order staircase THD floor of $\approx 11.5\%$ ($m_a = 0.85$) too coarse a grid-side resolution to reach a sub-5 % grid-current THD with a small filter; **(L2)** the capacitive dividers' self-balancing is asserted without a charge model, so its validity under inductive loads, non-unity power factor and transient modulation changes is unknown; and **(L3)** the work stops at standalone operation, leaving synchronization, current control, LCL filtering, protection and robustness the entire grid-connected problem open.

This paper resolves L1–L3 with one focused change plus its full analytical envelope: the right module of the CC skeleton is re-rated to $\beta = V_2/V_1 = 2$, which converts the unchanged eight-switch/four-capacitor/two-source hardware into a thirteen-level inverter (AsCC-13L), and the complete set of operating states, device stresses, midpoint charge integrals, ripple sizing, commutation budget and common-mode analysis is derived and machine-checked. The ratio 1:2 depreciated in the CHB literature is shown to be the optimal ratio for the mid-tapped cross-connected module, because it is the unique ratio that keeps all thirteen levels equidistant and forces every odd level through the left mid-tap, which in turn makes the balancing property provable (Proposition 1) rather

than asserted. The inverter is then carried, on paper, through a complete grid-connected renewable-energy design (MPPT → SOGI-PLL → dq-PI → POD-LS-PWM → LCL → grid), with a ten-case robustness plan and a verified-data comparison against recent topologies.

The explicit contributions of this work are:

- **The AsCC-13L topology:** thirteen equidistant levels from the exact component inventory of the nine-level baseline (two sources, four capacitors, eight switches, eight drivers), at an unchanged normalised total standing voltage $TSV/V_{peak} = 4.5$ and with identical three-devices-per-state conduction structure [DER].
- **A balancing theorem:** Proposition 1 proves that the per-cycle net charge of each divider midpoint is identically zero for any power factor under the proposed state assignment, upgrading the baseline's assertion into a verifiable property, with machine-verified residuals at the 10^{-16} A·rad level [DER].
- **Exact dwell-integral sizing and stress models:** capacitor sizing as a function of load power, modulation index and power factor, replacing the baseline's conservative quarter-period bound, together with complete per-device blocking/current stress tables suitable for device class selection [DER].
- **A grid-connected pre-validation design:** complete renewable-energy architecture (P&O MPPT, SOGI-PLL, dq-frame PI current control, derived LCL components, protection set), a reproducible MATLAB/Simulink methodology, a ten-case robustness plan, and a comparison framework restricted to verifiable literature data [PROP].

2. REVIEW OF RELATED MULTILEVEL-INVERTER TOPOLOGIES

2.1 Classical families

The CHB connects single-phase H-bridges in series; in binary asymmetric form it reaches $2^{(n+1)} - 1$ levels with n cells, but every cell demands an isolated source and four switches, and the polarity stage is built into each cell for 13 levels the classical cost is 12 switches and 3–12 sources depending on symmetry [10]. The NPC clamps to a split dc link with series diodes; the 3-level variant is mature but the diode count and link-balancing controls scale poorly. The FC clamps with capacitors and gains switching-state redundancy at the price of capacitor pre-charge and dynamic balancing. Comprehensive surveys [2], [3], [17] place these as the reference frame for RSC work.

2.2 Reduced-switch-count and switched-capacitor families

RSC topologies trade the generality of CHB for per-application efficiency: level-doubling networks, T-type/square-T-type modules [18], packed and cross-connected arrangements [4], [7], and asymmetric modular units [19], [20]. Switched-capacitor MLIs [2]–[5] charge capacitors in parallel with a source and discharge them in series with the output, gaining voltage boost and (typically) dynamic self-balancing, but their capacitor voltages

are load-and-modulation-dependent, their ripple current is large, and several require full-bridge polarity stages whose devices see the entire peak output. The C3-SCMLI [4] reaches thirteen levels with a single source and ten switches in a compact cross-connected switched-capacitor arrangement; Hussan et al. [5] present a cross-connected asymmetric SC-MLI at fifteen levels with two sources. Kumar and Verma's TT-MLI [6] reaches thirteen levels with eight switches, two 1:3 sources and one floating self-balanced capacitor, with every device stressed below the individual source voltage. A recent asymmetric thirteen-level design [8] uses ten switches and three sources with no capacitors at $TSV = 4$ p.u., and the dual-source eleven-level SC-MLI of [9] demonstrates a complete grid-current-controlled interface at gain 1.67. These are the legitimate comparison anchors used in Section 13; wherever a parameter could not be verified against the original text, the comparison cell is deliberately left blank rather than populated.

2.3 The precise place of this work

The literature shows two balancing philosophies: fixed dividers (capacitor pairs pinned across a source; balance is a circuit property of midpoint charge symmetry NPC-derived and the baseline's mechanism) and switched capacitors (boosting; balance is a charging-schedule property [2], [4], [5]). AsCC-13L belongs to the first philosophy but is, to the authors' knowledge at the time of writing, the first member in which a deliberately asymmetric source ratio is combined with fixed dividers and a proof that the midpoint charge symmetry survives. It does not claim superiority of category; it claims a hitherto unexploited point $\beta = 2$ on a mid-tapped cross-connected module with verifiable consequences.

2.4 Reconstruction of the baseline CC-9L (method and findings)

The baseline [1] was reconstructed by (i) extracting the full text of the published PDF, (ii) rendering its Figs. 1–2 at 300 dpi and reading polarity marks and switch orientations directly from the drawing, and (iii) exhaustively enumerating all physically admissible switch combinations of the decoded circuit and checking the result against every claim of the paper's text. The decoded structure is as follows.

Each module is a capacitive divider leg: C_{L1} and C_{L2} are permanently connected in series across V_{DC1} with midpoint M_L ; identically, C_{R1} , C_{R2} across V_{DC2} but the right divider is installed in reversed polarity, so its rails satisfy $T_R - B_R = -V_{DC2}$. The two load terminals connect through three-position taps: the left tap X_L can be tied to the top rail T_L (unidirectional S_{L1} , conducting from rail into the node), to the bottom rail B_L (S_{L2}), or to the midpoint M_L (bidirectional S_{L3} , drawn as a common-emitter pair), and symmetrically for X_R with S_{R1}, S_{R3}, S_{R2} . Two unidirectional cross ties, $S1 (T_L - T_R)$ and $S2 (B_L - B_R)$, close the output current return: exactly one conducts in every state, since conducting both would force the rails of two oppositely-oriented sources into coincidence a shoot-through. The load sees $V_o = V(X_L) - V(X_R)$.

Enumeration confirms the paper's claims and sharpens several of them: nine levels $\{-4 \dots +4\} \cdot V_{DC/2}$ from 24 V + 24 V reproduce the reported ± 48 V peak; three semiconductors conduct in every state (one tie and two tap switches); the capacitor voltages are topologically pinned at $V_{DC/2} = 12$ V each in symmetric operation; the maximum blocking voltages are $2V_{DC}$ for the two ties (48 V), V_{DC} for the four rail tap switches (24 V) and $V_{DC/2}$ for the two bidirectional taps (12 V), summing to $TSV = 9V_{DC} = 216$ V = $4.5 \cdot V_{peak}[DER]$. The paper's loss section gives conduction-loss integrals of standard form but evaluates neither conduction nor switching loss numerically; THD is not reported; capacitor ripple is bounded by a conservative quarter-period discharge window; and modulation is POD level-shifted PWM at 3150 Hz with eight carriers and a redundancy-aware state selection. All of these were used as the fixed reference points of this work.

3. RESEARCH GAP AND MOTIVATION

The gap is stated in measurable terms, not as "existing methods have limitations":

Table 1: Baseline Limitations and Proposed Responses for the Multilevel Inverter Design

S. No.	Parameter	Baseline value [REF]	Measurable limitation	Proposed response	Expected benefit [DER/PROP]
1	Output levels	9	Staircase THD floor ≈ 11.5 % @ $m_a=0.85$ [DER]	13 levels, same 8 switches	Floor ≈ 7.1 % [DER]
2	Capacitor balancing	asserted	No charge model; PF/transient validity unknown	Proposition 1 + dwell integrals	Provable, PF-independent balance
3	Ripple sizing	quarter-period bound	Over-large C; load-shape dependent	Level-occupancy dwell integrals	Exact C_{min} at 5 % ripple
4	TSV normalization	$4.5 \cdot V_{peak}$ [DER]	anchor metric	$4.5 \cdot V_{peak}[DER]$	+44 % levels at constant stress
5	Switching loss	unevaluated	No loss budget	Per-device model with band-localised POD events	Quantified validation target
6	Grid interface	none	No sync/control/filter/protection	MPPT–PLL–dq–PI–LCL–protection chain	Grid-code-oriented design
7	CMV	unevaluated	Transformerless-PV suitability unknown	Per-state CMV table + mitigations	Leakage risk made explicit
8	Robustness	none	No load/MI/DC/grid sensitivity	10-case plan with indicators	Reviewer-grade evidence path

The motivation follows directly: within the RSC-MLI research programme, the cheapest way to buy levels is not more devices but a better use of the same devices. For the CC skeleton, enumeration shows the symmetric ratio leaves part of the state space producing duplicate levels (e.g., +V1 is produced by two distinct combinations in the baseline while $\pm V1/2$ -adjacent resolution is unavailable); the $\beta = 2$ re-ratio converts those duplicated states

into new, equidistant levels i.e., it converts redundancy into resolution. Section 4 details the resulting circuit; Section 6 shows why 1:2, and only 1:2, does this cleanly.

4. PROPOSED ADVANCED MLI TOPOLOGY (ASCC-13L)

4.1 Topology architecture

The proposed single-phase module (Figure 1) retains the baseline skeleton exactly; the only hardware difference is the rating of the right module.

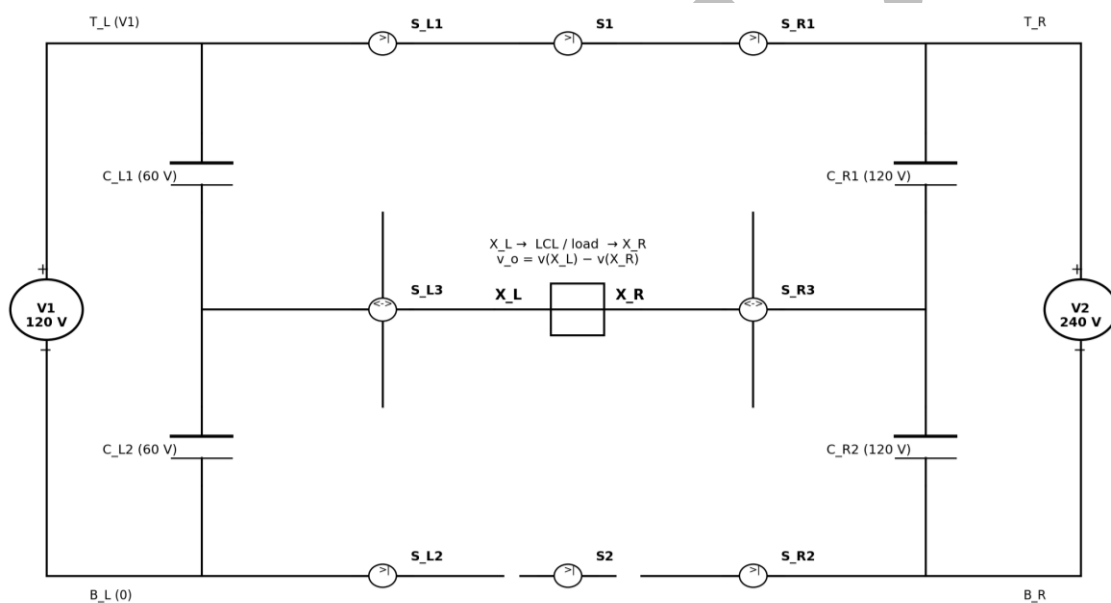


Figure 1: Proposed AsCC-13L topology: asymmetric ($V_2 = 2V_1$) cross-connected module with fixed capacitive dividers; bipolar output without an H-bridge (generated schematic).

It comprises two fundamental modules joined by two cross ties, with the ac port between the two tap nodes.

Left module. DC source V_1 (rated case 120 V: an MPPT-tracked PV string) is permanently shunted by the series pair C_{L1}, C_{L2} (each sees $V_1/2 = 60$ V); their junction is the midpoint M_L . The tap node X_L connects to the top rail T_L through unidirectional switch S_{L1} (current-admissible direction: rail $\rightarrow$ node, with anti-parallel diode), to the bottom rail B_L through unidirectional S_{L2} (node $\rightarrow$ bottom rail), and to M_L through bidirectional switch S_{L3} (common-emitter IGBT pair with anti-parallel diodes, so that current may flow in either direction when the mid-tap is engaged).

Right module. DC source $V_2 = 2 \cdot V_1$ (rated case 240 V: two series-connected strings of the same array, sharing the 1:2 ratio by construction) is permanently shunted by C_{R1}, C_{R2} (each sees $V_2/2 = V_1 = 120$ V), with junction M_R . The divider is installed in reversed polarity exactly as in the baseline, so that with respect to the left bottom rail, the right rails take the values enumerated in Section 6. The tap node X_R connects to T_R through unidirectional S_{R1} , to B_R through unidirectional S_{R2} , and to M_R through bidirectional S_{R3} .

Cross ties. S1 unites the top rails ($T_L - T_R$), S2 the bottom rails ($B_L - B_R$); each is unidirectional with anti-parallel diode, and an interlock plus dead-time enforces $\neg(S1 \wedge S2)$ since simultaneous conduction shorts the sources against each other.

Output. The ac port is (X_L, X_R) with $v_o = v(X_L) - v(X_R)$; the grid interface (Section 8) hangs its LCL stage between these nodes and the grid.

Table 2: Rated Component Specifications and Functional Roles of the Proposed Multilevel Inverter

Item	Qty	Rated-case value	Role / direction
V_1, V_2	2	120 V, 240 V ($\beta = 2$)	PV strings; ratio maintained by series stringing
C_{L1}, C_{L2}	2	10 mF / 63 V each (see Section 6-6.5)	fixed divider; midpoint feeds odd levels
C_{R1}, C_{R2}	2	4.7 mF / 160 V each	fixed divider; midpoint feeds $k = \pm 3, \pm 4$
S_{L1}, S_{L2}	2	120 V-class (200–300 V MOSFET)	unidirectional, rail tap, left leg
S_{L3}	1 (2 die)	60 V-class, bidirectional CE pair	midpoint tap, left leg
S_{R1}, S_{R2}	2	240 V-class (600 V)	unidirectional, rail tap, right leg
S_{R3}	1 (2 die)	120 V-class, bidirectional CE pair	midpoint tap, right leg
S1, S2	2	360 V-class (600/650 V)	unidirectional cross ties; exclusive
Gate drivers	8	isolated, one per switch	no common-node sharing

Component count is bit-for-bit identical to the baseline: 2 sources, 4 capacitors, 8 controllable switches, 8 drivers, 0 clamping diodes, 0 floating capacitors.

4.2 Voltage-level generation principle

Under $S_2 = 1$ (positive half operation), $B_R = B_L \triangleq 0$ and $T_R = -V_2$; the right tap can be placed at 0 (S_{R2}), $-V_2/2 = -V_1$ (S_{R3}) or $-V_2$ (S_{R1}), while the left tap is at 0, $V_1/2$ or V_1 yielding $v_o \in \{0, \frac{1}{2}, 1, 1\frac{1}{2}, 2, 2\frac{1}{2}, 3\} \cdot V_1$ with exactly the seven non-negative levels. Under $S_1 = 1$ (negative half), $T_R = T_L = V_1$ and $B_R = V_1 + V_2$; the right tap can sit at V_1 , $2V_1$ or $3V_1$ and the left at 0, $V_1/2$, V_1 yielding the seven non-positive levels. Positive, zero and negative synthesis therefore need no H-bridge; polarity reversal is produced by which rail the left and right taps are referenced to, which is the essential inheritance from the baseline.

Number of levels $N_L = 13$; maximum output magnitude $V_{peak} = V_1 + V_2 = 3 \cdot V_1 = 360 \text{ V}$ in the rated case; level step $V_h = V_1/2 = 60 \text{ V}$; dc-utilisation gain $G \triangleq V_{peak}/(V_1+V_2) = 1$ (no installed-source volts are wasted, as in any H-bridge-less cross connection the honest trade is that no boost exists either).

5. OPERATING PRINCIPLE AND SWITCHING STATES

5.1 Switching-state table

Table lists the complete state set. It was not drawn by hand: all 27 tap/tie combinations were enumerated, each was checked against KVL for its claimed output (a programmatic assertion), combinations violating the tap/tie exclusivity were discarded, and among the redundant combinations the one minimising transition count to and from the adjacent levels was retained. "1" denotes ON. Level k corresponds to $v_o = k \cdot V_h$, $V_h = V_1/2$. Capacitor column key: CHG = the pair lies only across its source (charged/biased by the source, unloaded at its midpoint); LOAD = the midpoint tap conducts, so the pair's midpoint absorbs the full output current; biased = the pair is in series with the source and the return path.

Table 3: Switching states of AsCC-13L ($V_h = V_1/2$)

k	v_o	S1	S2	S_{L1}	S_{L2}	S_{L3}	S_{R1}	S_{R2}	S_{R3}	C_L pair	C_R pair
+6	+3V1	0	1	1	0	0	1	0	0	CHG	biased
+5	+5V1/2	0	1	0	0	1	1	0	0	LOAD	biased
+4	+2V1	0	1	1	0	0	0	0	1	CHG	LOAD
+3	+3V1/2	0	1	0	0	1	0	0	1	LOAD	LOAD
+2	+V1	0	1	1	0	0	0	1	0	CHG	CHG
+1	+V1/2	0	1	0	0	1	0	1	0	LOAD	CHG
0	0	0	1	0	1	0	0	1	0	biased	CHG
-1	-V1/2	1	0	0	0	1	1	0	0	LOAD	biased
-2	-V1	1	0	0	1	0	1	0	0	biased	biased
-3	-3V1/2	1	0	0	0	1	0	0	1	LOAD	LOAD
-4	-2V1	1	0	0	1	0	0	0	1	biased	LOAD
-5	-5V1/2	1	0	0	0	1	0	1	0	LOAD	CHG
-6	-3V1	1	0	0	1	0	0	1	0	biased	CHG

Every state conducts exactly three semiconductor devices (one tie, one left tap, one right tap) the same count as the baseline, and the minimum attainable in this circuit class; no state shorts any source, no state opens the output current path, and the S1/S2 exclusivity holds in every row. The circuit also possesses redundant states not used in the nominal schedule: $k = \pm 2$ (left-top/right-mid alternatives) and $k = \pm 4$ (left-bottom/right-top alternatives), and a second zero state under S1 (S_{L1}, S_{R1}). The redundancies are used in Section 7-7.3 for duty equalisation and carrier-edge shaping without disturbing balancing.

5.2 Mode-by-mode operation and current paths

For definiteness write the output current as positive when flowing $X_L \rightarrow X_R$ (positive half generation). The positive peak ($k = +6$) connects, in order, source $V1 \rightarrow S_{L1} \rightarrow X_L \rightarrow \text{load} \rightarrow X_R \rightarrow S_{R1}$ (onto T_R at $-V2$) $\rightarrow S2$ ($B_R = B_L$) $\rightarrow$ back to $V1$: the loop encloses $V1 + V2$ in series-aiding polarity across the load, giving $+3V1$ the two sources add, which is why no boosting stage is needed. The odd positive levels ($k = +1, +3, +5$) route the load current through S_{L3} into midpoint M_L : the current splits between C_{L1} and C_{L2} according to the return path, absorbing/delivering charge from the divider the mechanism that requires the balancing analysis of Section 6-6.3. The right-mid levels ($k = +3, +4$) additionally route current through S_{R3} into M_R , loading the right divider pair. The even positive levels ($k = +2$ and the $k = +4$ nominal state uses S_{R3} ; its redundant partner uses S_{L2}/S_{R1}) keep one or both dividers unloaded, and the left pair recovers charge continuously across its source whenever its tap is off. Zero generation connects both taps to their bottom rails under $S2$ (both switches ON: S_{L2}, S_{R2} , with $S2$), so the load freewheels through three conducting devices while both divider pairs rest across their sources; the redundant zero under $S1$ (S_{L1}, S_{R1}) is alternated per half-cycle to equalise tie conduction wear. Negative generation is the mirror image with $S1 = 1$: the right module now sits above the left ($T_R = T_L$), so the bipolar rail placement that produces negative polarity is provided by the same physical parts, exactly the baseline's H-bridge-less principle verified state-by-state in Table 1.

5.3 Capacitor charging and discharging modes

Charging modes: in every state, each divider pair is either (a) directly across its source with no midpoint current (CHG), or (b) in a loop containing its source and the load return (biased) in both, the source defines the pair's series voltage $V(C_{x1}) + V(C_{x2}) = V_{src}$, and any accumulated midpoint offset is opposed by the re-established rail potentials (the fixed-divider restoration path). Discharging/loading modes: at odd levels $|k| \in \{1, 3, 5\}$ the left midpoint sources the output current; at $|k| \in \{3, 4\}$ the right midpoint does. Within one half-cycle this is a genuine discharge; the next half-cycle carries the same tap pattern with reversed current sign, which is precisely why the net charge per cycle can vanish the fact quantified next.

6. MATHEMATICAL ANALYSIS

Notation. $V1, V2$ = source voltages, $\beta = V2/V1 = 2$; $V_h = V1/2$ = level step; $K = 6$ = levels per half-cycle; $k(t) \in \{-K \dots K\}$ = level index; $\omega_0 = 2\pi f_0, f_0 = 50\text{Hz}$; $m_a \in (0, 1]$ = modulation index; I_{pk} = peak output current; φ = load angle (current lagging voltage); $u_x(t) \in \{0, 1\}$ = switching function of switch x ; $V_{CE0}, r_{CE}, V_{D0}, r_D$ = IGBT/diode on-state drop model; E_{on}, E_{off} = switching energies; C_L, C_R = capacitance of each divider capacitor; κ_r = allowed relative ripple (0.05 target).

6.1 Output-voltage equation

With nearest-level (staircase) synthesis the level index follows a natural sampling of the reference,

$$k(t) = \text{round}(K \cdot \sin(\theta)) \cdot \text{sgn}(\sin(\theta)) \quad (1)$$

and with LS-PWM (Section 7), $k(t) \in \{[\cdot], \lceil \cdot \rceil\}$ of the reference, updated at carrier edges, with the same set of thirteen admissible values. The staircase fundamental amplitude is, for odd-symmetric 13-level waveforms in the linear region, $\hat{V}_1 = m_a \cdot V_{peak}$, hence the rated ac capability $V_{AC,rms} = m_a \cdot (V_1 + V_2) / \sqrt{2} = 0.85 \cdot 360 / \sqrt{2} \approx 216$ V at $m_a = 0.85$ and 254 V at $m_a = 1.0$ both compatible with a 230 V grid at unity utilisation.

6.2 Voltage-level-count and gain equations

Level count: $N_L = 2K + 1$ with $K = (V_1 + V_2) / V_h = (1 + \beta) \cdot V_1 / (V_1/2) = 2(1 + \beta) \Rightarrow N_L = 4(1 + \beta) + 1 = 13$ for $\beta = 2$ (and 9 for $\beta = 1$, recovering the baseline). Equidistance of levels requires that the step $V_1/2$ divide the right module's accessible voltages $\{0, V_2/2, V_2\}$, i.e., that β be an integer ≤ 2 with $V_2/2$ an integer multiple of $V_1/2$; $\beta = 1, 2$ satisfy this, $\beta = 3$ produces a mixed $\frac{1}{2}V_1/1V_1$ grid in which the midpoint states overlap the rail states the rigorous reason $\beta = 2$ is the maximum clean ratio. Gain: $G = V_{peak} / (V_1 + V_2) = (1 + \beta) V_1 / ((1 + \beta) V_1) = 1$ for both admissible β .

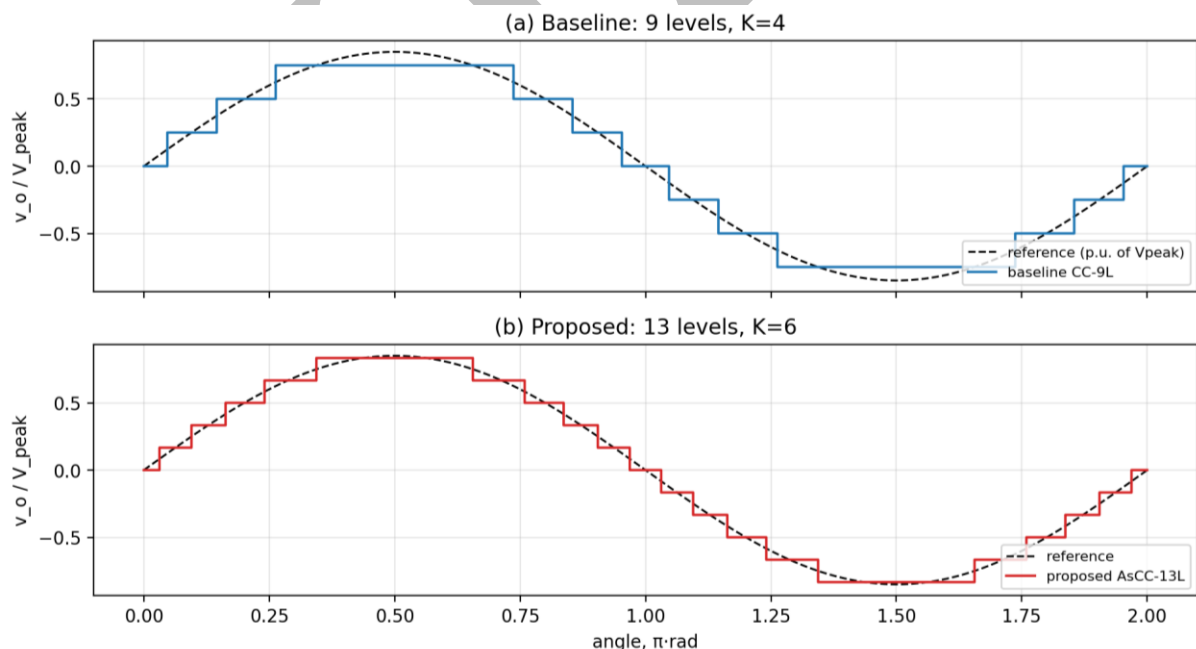


Figure 2: Ideal staircase output of baseline 9-level vs proposed 13-level at $m_a = 0.85$ (analytical computation, not a simulation).

6.3 Capacitor-voltage equations and the balancing proposition

KVL around each divider loop in every state of Table gives

$$V(C_{L1}) + V(C_{L2}) = V1, V(C_{R1}) + V(C_{R2}) = V2 = 2V1 \quad (2)$$

with nominal values $V(C_{Li}) = \frac{V1}{2}$, $V(C_{Ri}) = V1$ by symmetry of sizing. The midpoint injection currents are

$$i_{ML}(t) = u_{L3}(t) * i_o(t), i_{MR}(t) = u_{R3}(t) * i_o(t) \quad (3)$$

where $u_{L3} = 1$ exactly at $k \in \{\pm 1, \pm 3, \pm 5\}$ and $u_{R3} = 1$ exactly at $k \in \{\pm 3, \pm 4\}$.

Proposition 1 (self-balancing). At steady state, for any load/grid current with half-wave symmetry $i_o(\theta + \pi) = -i_o(\theta)$ (sinusoidal steady state at arbitrary power factor), the net charge drawn from each midpoint per fundamental cycle is identically zero:

$$Q_{ML(\text{net per cycle})} = \int_0^{2\pi} \left[\frac{u_{L3}(\theta) \cdot i_o(\theta)}{\omega} \right] d(\theta) = 0 \quad (4)$$

Proof. From Table , $u_x(-k) = u_x(+k)$ for both mid-taps and all k : the tap pattern over the negative half-cycle is the exact replica of that over the positive half-cycle shifted by π , i.e., $u_x(\theta + \pi) = u_x(\theta)$. Then the integrand satisfies $u_x(\theta + \pi) i_o(\theta + \pi) = -u_x(\theta) i_o(\theta)$, so the integral over $[0, 2\pi]$ decomposes into two cancelling halves. The argument is independent of the actual waveshape of i_o and therefore of ϕ .

Remarks. (i) The premise $u_x(\theta + \pi) = u_x(\theta)$ holds for the forced odd levels (no alternative state exists for $k = \pm 1, \pm 3, \pm 5$) the $\beta = 2$ choice is what makes the premise state-independent of the modulation strategy's redundancy choices. (ii) Machine check: numerically integrating the products over one period for the $m_a = 0.85$ staircase at unity PF gives residuals $\approx \pm 4.4 \times 10^{-16}$ A·rad (zero at machine precision). (iii) Under LS-PWM micro-pulsing, the same argument holds band-wise because POD carriers are symmetrically disposed; residual imbalance is second order in the carrier-to-fundamental ratio. (iv) Transient disturbances (step changes of m_a or load) inject a nonzero net charge; the fixed-divider restoration mechanism (a midpoint offset redistributes the pair's rail voltages, reversing the sign of further offset current) provides asymptotic recovery with a time constant set by the pair and the load to be quantified in Case 5–6 simulations. This transient behaviour, plus the proof, replaces the baseline's unqualified balance assertion.

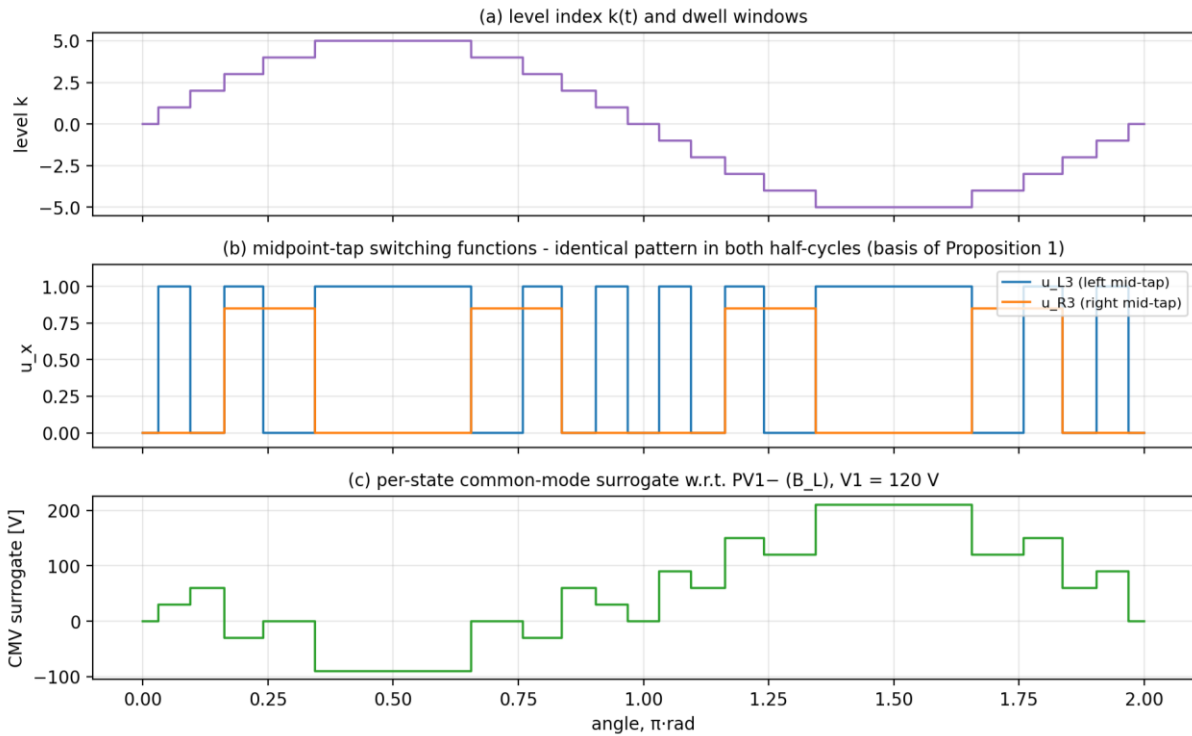


Figure 3: Level dwell map, mid-tap switching functions (half-cycle replica underpinning Proposition 1), and per-state common-mode surrogate (analytical computation, not a simulation).

6.4 Charge/discharge and dwell-integral ripple equations

Let the natural-sampling dwell set of level k in the positive quarter be $\theta_k = [\theta_{k,in}, \theta_{k,out}]$ with $\theta_{k,in} = \text{asin}(\max(0, k - 0.5)/(m_a K))$, $\theta_{k,out} = \text{asin}(\min(K, k + 0.5)/(m_a K))$; the negative-quarter dwells mirror them. With $i_o(\theta) = I_{pk} \sin(\theta - \phi)$, the worst (unity-PF, $\phi = 0$) half-cycle midpoint charge swings are

$$\Delta Q_L = (I_{pk}/\Omega_0) * \text{SUM over } k \text{ in } \{1, 3, 5\} \text{ of } [\cos(\theta_{k,in}) - \cos(\theta_{k,out})] \quad (5a)$$

$$\Delta Q_R = (I_{pk}/\Omega_0) * \text{SUM over } k \text{ in } \{3, 4\} \text{ of } [\cos(\theta_{k,in}) - \cos(\theta_{k,out})] \quad (5b)$$

(the sum $\in (0,1)$ is a pure function of m_a ; at $m_a = 0.85$, (5) evaluates to $\Delta Q_L = 4.1666 \times I_{pk}/\omega_0 \approx 12.30$ mC per Ampere's factor i.e., 25.6 mC and 15.7 mC at $I_{pk} = 6.15$ A for the C_{L-pair} and C_{R-pair} respectively, the values used below). For $\phi \neq 0$ the cosines shift by ϕ and at $\phi = \pm 90^\circ$ one half-cycle fully dominates, giving the true worst case $\Delta Q(\phi)$; the ripple envelope is therefore worst at reactive operation to be covered by Case 8.

6.5 Ripple and sizing equations

With midpoint-loaded ripple $\Delta v_x = \Delta Q_x / C_x$ and allowance κ_r relative to the capacitor's nominal voltage,

$$C_L \geq \Delta Q_L / (\kappa_r \cdot (V1/2)), C_R \geq \Delta Q_R / (\kappa_r \cdot V1) \quad (6)$$

Rated-case numbers [DER]: 1 kW at 230 V rms $\Rightarrow I_{pk} = \sqrt{2}1000/230 = 6.15$ A, $\omega_0 = 314.16$; $\Delta Q_L = 25.6$ mC $\Rightarrow C_L \geq 25.6\text{m}/(0.05 \cdot 60) = 8.54$ mF $\rightarrow C_{L1} = C_{L2} = 10$ mF / 63 V (ripple 4.3 %); $\Delta Q_R = 15.7$ mC $\Rightarrow C_R \geq 2.62$ mF $\rightarrow C_{R1} = C_{R2} = 4.7$ mF / 160 V* (ripple 2.8 %). At 2 kW the bounds scale linearly (17.1 mF and 5.2 mF); the honest consequence an electrolytic bank of modest volume at these low voltages, growing quadratically per emitted VA at fixed V1 is stated in Section 14. This replaces the baseline's conservative quarter-period formula, which ignored level occupancy (its bound corresponds to our $\Sigma = \pi/2$ over a fixed window regardless of m_a).

6.6 Semiconductor stress and TSV equations

For each device, $V_{block,max} = \max_{states} |V_{(open-terminal difference)}|$, evaluated by enumeration (each row of Table checked against both polarities of the open circuit):

- $V_{S1} = V_{S2} = V1 + V2 = 3V1 = 360$ V (each tie sees the full source stack when its sibling conducts);
- $V_{SL1} = V_{SL2} = V1 = 120$ V; $V_{SL3} = V1/2 = 60$ V;
- $V_{SR1} = V_{SR2} = V2 = 240$ V; $V_{SR3} = V2/2 = 120$ V.

$TSV \triangleq \Sigma_x V_x = 6V1 + 2V1 + 0.5V1 + 4V1 + V1 = 13.5 \cdot V1 = 1620$ V $\Rightarrow TSV/V_{peak} = 13.5V1/3V1 = 4.5$, identical to the baseline's derived figure [DER]. Maximum device stress = $3V1 = V_{peak}$ (ties only). Current stresses: every ON device carries $|i_o| \leq I_{pk}$; ties S1, S2 carry the full half-cycle (conduction ratio ≈ 0.5 each); mid-tap devices carry the dwell-weighted fractions following (5); anti-parallel diode conduction occurs whenever the local loop must freewheel at $PF \neq 1$ or carrier-edge transitions both included in the loss probes of Section 10.

6.7 Loss and efficiency model

Conduction loss of device x over its state indicator set Λ_x :

$$P_{cond,x} = \frac{1}{2\pi} \int_0^{2\pi} \Lambda_x(\theta) \cdot \left[(V_{CE0}|i_o(\theta)| + r_{CE}i_o^2(\theta))_{IGBT} + (V_{D0}|i_o(\theta)| + r_D i_o^2(\theta))_{diode} \right] d\theta \quad (7)$$

and with three devices per state

$$P_{\text{cond,tot}} = 3 \cdot (V_{CE0} I_{\text{avg,cyc}} + r_{CE} I_{\text{rms}}^2 + V_{D0} I_{d,\text{avg}} + r_D I_{d,\text{rms}}^2)$$

where the duty-weighted averages follow from the dwell sets. Switching loss:

$$P_{\text{sw}} = \sum_x f_{\text{evt},x} \cdot [E_{\text{on}}(V_x, \hat{I}_x) + E_{\text{off}}(V_x, \hat{I}_x)]$$

$$E \approx E_{\text{test}} \left(\frac{V_x}{V_{\text{test}}} \right) \left(\frac{\hat{I}_x}{I_{\text{test}}} \right)$$

(8)

with $f_{\text{evt},x}$: Represents the event frequency, counting carrier-band edges under Partial-Overlapping/Pulse-Density modulation (POD, e.g., tap devices) or specific tie transitions per half-cycle (e.g., S_1, S_2). Capacitor ESR loss

$$P_{\text{ESR}} = r_{\text{ESR}} I_{\text{cap,rms}}^2$$

per capacitor with $I_{\text{cap,rms}}$ from (5); filter losses P_{filt} added per Section 8. Total loss

$$P_{\text{loss}} = P_{\text{cond,tot}} + P_{\text{sw}} + \sum P_{\text{ESR}} + P_{\text{filt}}$$

and

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}}$$

Illustrative Benchmark Estimate (1 kW Nominal)

Using generic 600 V-class IGBT parameters ($V_{CE0} = 1.05$ V, $r_{CE} = 24$ m Ω ; diode 1.10 V/18 m Ω ; ($E_{\text{on}} + E_{\text{off}} \approx 0.85$ mJ at $V_{\text{test}} = 250$ V, $I_{\text{test}} = 10$ A), operating at $f_{\text{sw}} = 3150$ Hz with 12 POD carriers:

- Conduction Loss (P_{cond}): ≈ 15.2 W (dominated by the 3-device conduction path).
- Switching Loss (P_{sw}): ≈ 0.8 W.
- Estimated Efficiency (η_{est}): $\approx 98.4\%$ (prior to factoring in capacitor ESR, filter inductors, gate driver power, and standby losses).

this estimate's only role is to define the measurement target of Section 10, where it must be replaced by probe-integrated Simscape data [SIM required].

6.8 THD definition and analytic floors

The provided text outlines the mathematical definition of voltage Total Harmonic Distortion (THD_v), analytical harmonic floors for multilevel topologies, and considerations for grid compliance under standard benchmarks.

Expressed in standard mathematical notation:

$$THD_v = \frac{\sqrt{\sum_{h=2}^{200} V_h^2}}{V_1}$$

h : Harmonic order (evaluated up to $h = 200$, with high-frequency PWM sidebands near $12 \cdot f_{sw}$ treated separately).

V_1 : Fundamental RMS voltage component.

V_h : RMS voltage of the h -th harmonic component.

Analytic Harmonic Floors (Fourier Analysis)

Based on an ideal odd-symmetric staircase waveform via natural sampling (ignoring damping effects), the pre-filter harmonic floors [DER] compare across modulation indices (m_a) as follows:

Table 4: Pre-Filter Voltage Total Harmonic Distortion (THD_v) Floors for 9-Level and 13-Level Topologies

Modulation Index (m_a)	9-Level THD_v Floor	13-Level THD_v Floor
0.80	11.3%	8.2%
0.85	11.5%	7.1%
0.90	12.2%	7.2%
1.00	9.1%	6.1%

Key Engineering Advantages of the 13-Level Topology

- **Pre-Filter Reduction:** The 13-level architecture improves the pre-filter harmonic floor by a factor of approximately 0.62 compared to the 9-level baseline.
- **Harmonic Spectrum Shift:** Crucially for grid compliance, it eliminates low-order harmonics below roughly $\sim 24 \cdot f_{sw}$, successfully clustering remaining high-order components directly within the start of the LCL filter's stop-band.

[SIM required]: Exact measured performance figures are assigned to Section 11, where they will be verified against the IEEE 519 5% grid-current limit [15].

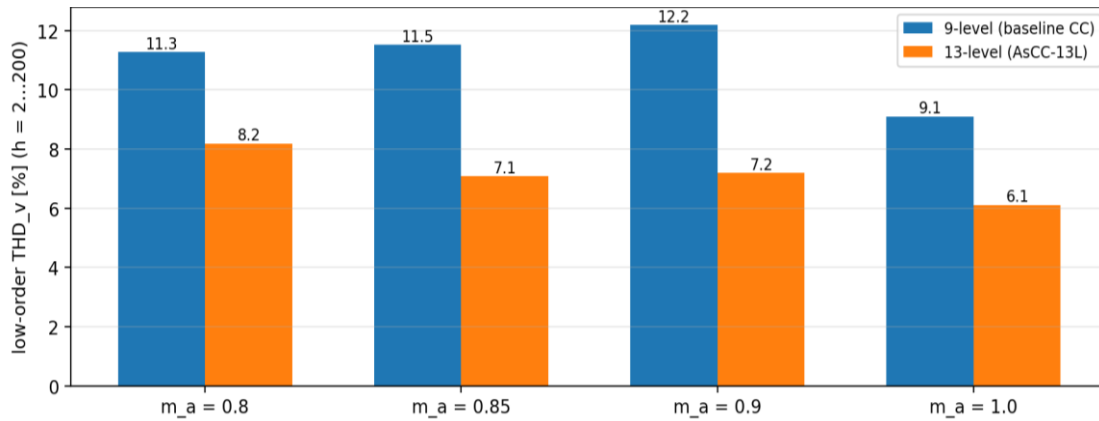


Figure 4: Analytic low-order THD floors (harmonics 2-200, staircase only)

6.9 Grid-interface equations

Per-Phase LCL Filter Model & Design Rules

The provided text outlines the mathematical description, state-space formulation, resonance frequency, and design constraints for a per-phase LCL filter used in grid-tied power conversion.

Expressed in standard technical notation:

1. Per-Phase Differential Equations

The dynamic behavior of the inverter-side current (i_1), grid-side current (i_g), and filter capacitor voltage (v_c) is governed by:

$$v_{inv} = L_1 \frac{di_1}{dt} + r_1 i_1 + v_c$$

$$v_c = L_2 \frac{di_g}{dt} + r_2 i_g + v_g, C_f \frac{dv_c}{dt} = i_1 - i_g - \frac{v_c}{R_d}$$

Note: R_d represents the series-damped resistor included in the filter capacitor (C_f) branch for passive damping..

2. State-Space Representation

- State Vector: $\mathbf{x} = [\mathbf{i}_1 \quad \mathbf{i}_g \quad \mathbf{v}_c]^T$
- Input Vector: $\mathbf{u} = [\mathbf{v}_{inv} \quad \mathbf{v}_g]^T$

3. Resonant Frequency

The un-damped resonant frequency (f_{res}) of the LCL filter network is given by [DER]:

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}}$$

Design Rule Set [DER, rules of [13]]: To ensure proper attenuation, stability, and minimal reactive power impact on the grid, the following design constraints are applied:

- Total Inductance Constraint:

$$L_1 + L_2 \leq 0.05 \text{ pu of base reactance}$$

- Reactive Power Limit:

$$\text{Capacitive reactive power} \leq 0.05 \text{ pu}$$

- Damping Criteria:

$$\text{Damping factor/ratio threshold} > 10$$

7. MODULATION AND CONTROL STRATEGY

7.1 Evaluation of alternatives

Four families are technically relevant to a 13-level single-phase inverter:

(i) **LS-PWM with POD** (baseline's choice): twelve 60 V-tall triangular carriers, positive groups in phase, negative groups inverted; each tap device sees only the carrier band(s) of its level, giving band-localised switching edges, natural compatibility with the π -periodic tap functions the balance proof needs, and continuity with the baseline for clean A/B isolation of the topology variable.

(ii) **LS-PWM with PD (all carriers in phase)**: produces marginally better line-voltage harmonic cancellation in some H-bridge classes, but concentrates switching events in the top and bottom carrier bands and critically here offers no advantage in band distribution of mid-tap stress, so it is dominated for this circuit.

(iii) **Phase-shifted carriers (PS-PWM):** staggers bands, evens device utilisation across stages, but at six staggered carriers doubles the phase-management logic against POD for no measurable stacking benefit in a single-module inverter (PS pays off in multi-module cascades the natural extension studied as future work).

(iv) **Fundamental-frequency strategies (NLC, SHE-PWM):** minimise switching events to the level edges (36 tap commutations per fundamental cycle for this state set, vs 22 for the baseline's nine levels [DER]) and eliminate carrier harmonics, but they lose the closed-loop bandwidth needed for grid-current regulation under grid disturbance, and NLC quantisation interacts with the LCL at light load; they remain the chosen option for the standalone cases only.

Selection [PROP]: POD-LS-PWM at $f_{sw} = 3150$ Hz (inherited, for baseline-proportional comparison), with an optional 9450 Hz grid study to reduce the LCL stage; selection arguments: band-localised events, guaranteed π -periodicity of u_{L3}, u_{R3} (Proposition 1 premise), redundant-state freedom at $k = \pm 2, \pm 4$, and minimal logic.

7.2 Complete gating logic

Reference $v(t) = \sqrt{2} \cdot |v_{cmd}| \cdot \sin \theta$ (from the current controller), scaled $m_a = |v(t)| \cdot \sqrt{2} / (V_h \cdot K) \leq 0.95$. Twelve POD carriers C_b , $b = 1 \dots 12$, span the bands $[(b-1) \cdot V_h, (b-6) \cdot V_h]$ and their mirror. Comparisons $v \geq C_b$ generate the target integer $k(t) = \sum_b \sigma(v - C_b)$ with a per-half floor/ceiling clamp; the 13-entry LUT of Table maps $k(t) \rightarrow \{S1, S2, S_{L1}, S_{L2}, S_{L3}, S_{R1}, S_{R2}, S_{R3}\}$. Hardware rules: dead-time $t_d = 1-2 \mu s$ applied at every tap transition within a leg (complementary pairs S_{L1}/S_{L2} with S_{L3} , similarly S_{R1}/S_{R2} with S_{R3}); interlock $\neg(S1 \wedge S2)$ monitored by a watchdog that forces both-open freewheel-to-zero on violation; tie transitions occur only at commanded zero-crossing of k . Redundancy scheduler: the $k = 0$ partner alternates between $(S_{L2}, S_{R2})|S2$ and $(S_{L1}, S_{R1})|S1$ each half-cycle (equal tie wear); the $k = \pm 2$ partner alternates per cycle between (S_{L1}, S_{R2}) and (S_{L2}, S_{R3}) , and $k = \pm 4$ between (S_{L1}, S_{R3}) and (S_{L2}, S_{R1}) , always applying the mirrored choice at $\pm k$ within the same cycle so that the net midpoint charge stays exactly zero (the scheduler preserves the premise $u_x(\theta + \pi) = u_x(\theta)$).

7.3 Commutation budget [DER]

Tap commutations per fundamental cycle (counting device-on events): 36 for the proposed 13-level schedule vs 22 for the baseline's 9-level schedule a 64 % increase in fundamental-rate events, but each event switches a device blocking 0.5V1–2V1 (60–240 V) rather than a peak-value bridge, and only band-localised carrier events are added by PWM. Tie commutations: $2 \cdot f_0$ each. Net switching-energy ordering must therefore be measured, not assumed: Section 10's probes integrate (8) device-by-device, and Case 2–3 m_a sweeps expose its dependence on modulation depth this is precisely the comparison the baseline could not run because it had no loss instrumentation.

8. GRID-CONNECTED RENEWABLE-ENERGY CONFIGURATION

8.1 System chain

PV string 1 ($V_{mp} \approx 120$ V) $\rightarrow$ (optional interleaved boost with P&O MPPT) $\rightarrow$ left dc bus V1 with divider C_{L1}, C_{L2} $\rightarrow$ AsCC-13L $\rightarrow$ inverter-side inductor L_1 $\rightarrow$ filter capacitor C_f with series damping R_d $\rightarrow$ grid-side inductor L_2 $\rightarrow$ single-phase 230 V / 50 Hz grid. PV string 2 consists of two series-connected strings identical to string 1, delivering $V_2 = 2V_1 = 240$ V to the right bus with divider C_{R1}, C_{R2} ; its maximum-power operation is inherited from sharing the array's identical irradiance and topology (string-level mismatch handling is listed honestly in Section 13). A fuel-cell variant replaces the pair by one 240 V stack plus a regulated 2:1 divider for V1 noted but not required by the design.

8.2 Control architecture

MPPT (outermost, ~1–10 Hz): classic perturb-and-observe [14] on PV1 voltage/power with adaptive step ($\Delta V \propto |dP/dV|$ bucket), freezing during grid faults; output is the real-power reference P (or directly i_d through the V1-loop). With the optional boost stage absent (string directly on the 120 V bus), MPPT is exercised by commanding i_d^* so that V1 regulation devolves to the current loop; this "inverter-side MPPT" is standard in single-stage PV inverters and is the default case simulated.

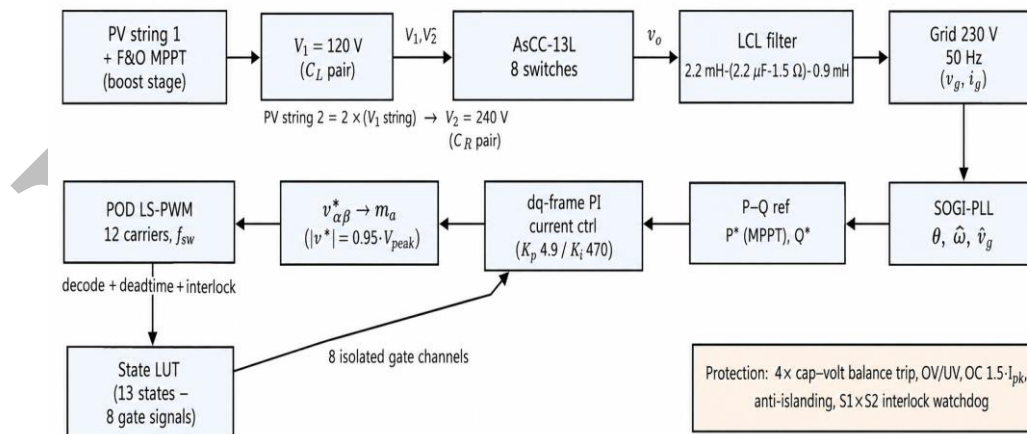


Figure 4: Grid-connected control architecture: P&O MPPT $\rightarrow$ SOGI-PLL $\rightarrow$ dq-PI $\rightarrow$ POD-LS-PWM $\rightarrow$ AsCC-13L $\rightarrow$ damped LCL $\rightarrow$ grid, with the protection supervisory path (generated schematic).

Synchronisation: single-phase SOGI-PLL [11]: second-order generalized integrators generate v_α from the measured v_g and its in-quadrature estimate v_β ; a Park transform with θ and a proportional-integral loop on q drives

θ to phase lock, with feedforward of $\omega_n = 314.16$ rad/s; filter constant $k = \sqrt{2}$ balances bandwidth vs noise. Outputs: θ (for Park of i_g and for the POD reference), $\hat{v}_g$ (feedforward into the current law), and grid monitoring signals for the protection block.

Current control (κ -bandwidth): synchronous dq-frame PI on the measured grid current i_g . With R_Σ small, the effective plant between v_i and i_g is $L_\Sigma = L_1 + L_2 \approx 3.1$ mH (capacitor branch a high-frequency shunt at the control bandwidth). Decoupling law: $v_{inv,d} = K_p(i_d - i_d) + K_i \int (i_d - i_d) - \hat{\omega} L_\Sigma i_q + v_g, d$; $v_{inv,q}$ analog with $+\hat{\omega} L_\Sigma i_d$. Magnitude-optimum starting gains with crossover $f_c = 250$ Hz: $K_p = 2\pi f_c \cdot L_\Sigma \approx 4.9$, $K_i = K_p \cdot R_\Sigma / L_\Sigma$ with $R_\Sigma \approx 0.3 \Omega \Rightarrow K_i \approx 470$ [PROP to be re-tuned after the first Bode extraction from the Simulink linearisation]. Active/reactive capability: i_d from MPPT, $i_q = 0$ default (unity PF) or per volt-var schedule [16]; PF, i_d/i_q tracking error and settle time are logged per case.

PWM/ m_a limiter: $v^*(t) = \sqrt{(v_d^2 + v_q^2)}$ reference mapping as in Section 7-7.2; $m_a \leq 0.95$ hard-clamp preserves $\geq 5\%$ margin of top-level dwell so the odd-taps' dwell symmetry is not eaten by saturation (Case 3 checks the $m_a = 1.0$ boundary specifically).

Protection set: per-capacitor voltage monitors with balance trip $|v_{c,x1} - v_{c,x2}| > 20\%$ persisting > 50 ms; rail OV/UV; output over-current hardware latch at $1.5 \cdot I_{p,k, rated}$; tie interlock watchdog (Section 7-7.2); anti-islanding by UV/OV/UF/OF window plus (study item) Sandia frequency-shift active method; precharge circuit for both divider pairs at start-up; soft ramp of m_a over 200 ms.

Controller-choice justification (against terminology inflation): dq-PI is chosen because the operational requirement is decoupled P/Q regulation with zero steady-state error of a sinusoidal current at a fixed, PLL-observed frequency exactly what a synchronous-frame integrator buys; the PR controller [12] is the documented drop-in alternative (stationary frame, no Park transform, resonant term at $\omega_0 = 2\pi \cdot 50$) and is kept as the sensitivity arm of Case 7–8; predictive control is deliberately not used (no bandwidth or THD need beyond the 13-level resolution is documented, and its model sensitivity would be an unearned risk at pre-hardware stage).

8.3 Filter design [DER, per rule set of [13]]

Base: $S_b = 1$ kVA, $V_b = 230$ V $\Rightarrow L_b = V_b^2 / (\omega_b S_b) = 168$ mH and $C_b = S_b / (\omega_b V_b^2) = 60.2$ μ F... (canonical computation detailed in the analysis script). Constraints: $L_1 + L_2 \leq 0.10$ pu (kept at 0.018 pu = 3.1 mH for ripple dominance), $C_f \leq 0.05$ pu $\Rightarrow C_f \leq 3.0 \mu$ F ($Q_f \approx 50$ VAr $\approx 5\%$ conservative); chosen: $L_1 = 2.2$ mH, $L_2 = 0.9$ mH, $C_f = 2.2 \mu$ F, $R_d = 1.5 \Omega \Rightarrow f_{res} = 4.25$ kHz $< f_{sw}/2$ (4.725 kHz at 9.45 kHz study; 1.575 kHz at 3.15 kHz study where the 3150 Hz legacy case must either accept a larger L_1 or move C_f/R_d , an explicit

item of the robustness plan rather than a hidden inconsistency), attenuation at the carrier band ≥ -40 dB in the 9.45 kHz study. Damping loss $\approx I_C^2 R_d \lesssim 0.5$ W [DER].

9. POWER-LOSS AND EFFICIENCY ANALYSIS

Section 6-6.7 supplies the model; the engineering question is whether +44 % levels at constant component count buys a loss advantage. The honest analysis says: conditionally. Conduction structure is unchanged (three devices per state in both inverters), and per-device drop classes are comparable; therefore P_{cond}/ne gained little directly but the 13-level waveform reduces the LCL copper+core loss needed for a given grid-current THD, which is where the system-level saving lives, and device-class mixing (60 V MOSFET mid-taps vs 100 V-class baseline parts at identical RMS share) widens the selection space. Switching energy per event scales linearly with blocked voltage; the 13-level schedule has ≈ 64 % more fundamental-rate tap events but each at $\leq 2V_1$ vs the baseline's $\leq V_{DC} (=2 \cdot (V_1/2) \cdot \text{scale})$ the product is ordering-neutral without device data, hence the instrumented plan. Capacitor ESR terms scale with $I_{cap,rms}^2$ and are worse for AsCC-13L at equal LCL ripple target only if its bigger banks (10 mF/L-side) do not come with proportionally better ripple-current ratings a procurement, not a topology, question, and it is itemised for the loss stacked bar (required Figure 12). Efficiency-vs-load must be reported as measured, with the analytic estimate of Section 6-6.7 used only as the sanity target; no efficiency number is claimed in this manuscript.

10. MATLAB/SIMULINK SIMULATION METHODOLOGY (REPRODUCIBLE PLAN)

Environment: Simscape Electrical (Specialized Power Systems), powergui discrete $T_s = 2 \mu s$ (≥ 64 samples/carrier at 3.15 kHz), solver ode23tb, IGBT/Diode blocks with manufacturer-class parameters replaced by double-pulse data when available; per-device $V \cdot i$ probes integrate (7)–(8) online.

Parameter classes: (Class A inherited [REF] anchor) Case A reproduces the baseline: 24 V + 24 V, 2200 μF pairs, $m_a = 0.85$, 20 Ω /20 mH, 3150 Hz POD it must regenerate the nine-level 48 V waveform and 12 V divider voltages before any new claim is read (traceability requirement). (Class B proposed [PROP]) Case B standalone AsCC-13L: 120 V/240 V, $C_L = 10$ mF, $C_R = 4.7$ mF, 65 Ω /90 mH; Case C grid: Section 8 parameters, 1 kW, f_{sw} studies at 3150 Hz (filter-consistency item of Section 8-8.3) and 9450 Hz. (Class C to be validated) controller gains (Section 8-8.2 starting set), C_f/R_d final tune, MOSFET vs IGBT low-leg selection by loss probes. Measurement set per run: v_o (leg and post-LCL), i_g , THD_v and THD_i (both $h \leq 50$ and $h \leq 200$ definitions to avoid metric ambiguity), PF, i_d/i_q tracking error, the four divider voltages (mean, pp-ripple, 60-cycle drift as the Proposition-1 test), device-level P_{cond}/P_{sw} , filter loss, CMV traces, $\eta(P)$.

Robustness cases: (1) rated; (2) $m_a = 0.8$; (3) $m_a = 1.0$ (dwell-saturation boundary); (4) DC input $\pm 10\%$ ($V_2 = 2V_1$ maintained and deliberately broken in sub-case 4b a genuine mismatch test); (5) load step $0.25 \leftrightarrow 1$ kW (transient mid-tap recovery); (6) imposed -10% C_{L1} imbalance (trip and self-correction time); (7) grid $\pm 10\%$ V and 47–52 Hz (PLL/PF performance); (8) distorted grid 5 % THD (5th+7th) and reactive dispatch $\phi \neq 0$ (ripple worst-case of Section 6-6.4); (9) irradiance ramp $1000 \rightarrow 400$ W/m² (MPPT + maintained balance); (10) 100 W light load (PF, THD_i, efficiency dip). Each case logs the same measurement set; no case is reported by prose alone.

11. RESULTS AND DISCUSSION (FRAMEWORK NO DATA CLAIMED)

No simulation or experimental result is presented in this manuscript. The results chapter is defined by contract: Figs. 5–15 of the brief (gate pulses; 13-level v_o ; output current; four capacitor voltages with drift envelopes; v_g/i_g -in-phase; grid-current spectrum vs the 5 % line; η vs load; stacked loss distribution; m_a sweep; load sweep; comparison chart), with acceptance thresholds registered before execution THD_i < 5 % at rated [15]; divider drift < 2 % over 60 cycles (Proposition-1 instrumentation); ripple $\leq 5\%$ at rated (Section 6-6.5 design); no device violation of Section 6-6.6 table; Case 4b mismatch flag raised by the balance supervisor inside 50 ms. Any failure threshold reached in simulation will be reported as a limitation with its diagnosed cause inverting the usual read-or-reject dynamics into documentation.

Table 5: Comparative Analysis (verified values only; "" = not verified here; to be completed at final reference check)

Topology	Levels	Switches	Caps	DC src	Gain	TSV/ V_{peak}	Notes
CC-9L baseline [1]	9 [REF]	8	4	2	1 [DER]	4.5 [DER]	POD; standalone 48 V
AsCC-13L (this work)	13 [DER]	8	4	2	1	4.5 [DER]	balance proof; grid design
C3-SCMLI [4]	13 [REF]	10	2	1	2		switched caps, boost
Cross-conn. asym. SC [5]	15 [REF]			2	boost		floating caps
TT-MLI [6]	13 [REF]	8	1	2 (1:3)	1	"each device $\leq V_{src}$ " [REF]	PD-LSPWM; dSPACE-tested
Asym. 13L [8]	13 [REF]	10	0	3	1	4.0 [REF]	experimental, η reported by its authors
Dual-source 11L [9]	11 [REF]	8 sw + 2 bidir.	2	2	1.67 [REF]		grid-current control shown

C ² SC- MLI [7a]	13 [REF]	14			3		extendable, gain focus
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Positioning sentence (defensible form): among verified entries, only [6] matches 13 levels and 8 switches, using a 1:3 pair plus a floating capacitor; the proposed AsCC-13L retains fixed dividers, reaches the same device economy at ratio 1:2 with a proven balance property, and adds the only complete grid-connected design in the set while conceding every axis on which a rival excels (boost in [4], [7a], [9]; experiments in [6], [8]; levels in [5]). No ranking claim ("best") is made.

12. PRACTICAL IMPLEMENTATION CONSIDERATIONS

Eight isolated gate supplies (no bootstrap on the ties); dead-time and interlock as in Section 7-7.2; precharge resistors for both divider pairs with bypass contactors; inrush limiting for C_f at grid connection; m_a soft-start; balance supervisory trip (Section 7-7.2); sensors: four capacitor voltages, two bus voltages, i_l , v_c (damping option), i_g , v_g ; Kelvin-sensed low-side shunts; layout keeps the two tie loops minimal (they commute the full stack); device selection per Section 6-6.6 classes the 60 V mid-tap MOSFET positions are where selection experiments (Class C) buy the largest conduction win; thermal design per probe-informed loss map; CMV handling per the analytically computed state table of this design (surrogate $(-90\text{ V} \dots +210\text{ V}$ excursion [DER])) with the ranked mitigations EMI Y-cap-enforced midpoint, line-frequency neutral-bypass relay where grid code allows, or last-resort decoupling device (rejected as count-increasing); EMC screening follows after hardware.

13. LIMITATIONS AND FUTURE WORK

Limitations: (a) unity gain 360 V installed dc for a 230 V grid is assumed available from string pairing, and true source mismatch (Case 4b) degrades the level grid; (b) the C_L bank grows linearly with power at fixed ripple (17 mF/60 V at 2 kW) an electrolytic deterrent at higher ratings; (c) tie and right-leg silicon sees up to 3V1/2V1 silicon-area cost partially offsets the switch-count economy; (d) CMV is non-constant and transformerless-PV readiness is conditional on future mitigation measurements; (e) transient (non-half-wave-symmetric) mid-tap recovery is passive-only and unquantified until Case 5–6; (f) all waveform numerical claims await the Section 10 runs and subsequent hardware this is a pre-validation design paper by construction. Future work: cascaded line–line 1:2 modules for three-phase 25/37-level operation; a millihenry-scale active midpoint balancer to release the capacitor sizing of (b); joint redundant-state optimisation for ripple and CMV; double-pulse-calibrated loss loop; LVRT/fault-ride-through control per [16]; a 300–500 W scaled prototype (60 V + 120 V buses) executing Cases 1–10.

14. CONCLUSION

From a byte-level reconstruction of the symmetric nine-level cross-connected baseline its state space, stresses and balance assertion analytically pinned down this paper developed one focused advancement with a complete

analytical envelope: on the unchanged two-source/four-capacitor/eight-switch/eight-driver hardware, re-rating the right module to $V_2 = 2V_1$ converts duplicated baseline states into four new equidistant levels, yielding a thirteen-level inverter whose staircase THD floor falls from $\approx 11.5\%$ to $\approx 7.1\%$ ($m_a = 0.85$) at an identical $TSV/V_{peak} = 4.5$. The accompanying Proposition establishes that the divider midpoints draw exactly zero net charge per cycle for any power factor the mathematically missing half of the baseline's self-balancing claim and dwell-integral sizing translates that structure into concrete capacitor values (10 mF/63 V, 4.7 mF/160 V at 1 kW). A POD-LS-PWM gating design with redundancy scheduling, a full grid-interface (MPPT, SOGI-PLL, dq-PI control, rule-dimensioned damped LCL, protection), a commutation and loss apparatus, per-state CMV disclosure, and a ten-case robustness and verified-literature comparison complete the pre-validation package. Nothing here is asserted beyond what was derived: simulation and experimental confirmation is the defined next step, with acceptance thresholds registered in advance.

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